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**Code No. : 14668 N/O**

# VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

*Accredited by NAAC with A++ Grade*

## B.E. (I.T.) IV-Semester Main & Backlog Examinations, July/August-2023

## Computer Organization

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

***Part-A (10 × 2 = 20 Marks)***

| Q. No. | Stem of the question | M | L | CO | PO |
|---|---|---|---|---|---|
| 1. | Discuss the significance of PC and IR registers. | 2 | 2 | 1 | 1 |
| 2. | With a neat diagram, differentiate between Big endian and Little endian memory addressing. | 2 | 2 | 1 | 1 |
| 3. | Perform arithmetic left shift operation and logical left shift operation on the following data.<br>a) 10011001 b) 10110011 | 2 | 3 | 2 | 2 |
| 4. | "Microprogrammed control is more flexible than Hardwired control". Is the statement true or false. Justify. | 2 | 3 | 2 | 1 |
| 5. | What is cycle stealing? | 2 | 1 | 3 | 1 |
| 6. | What is the need of an Input-Output Interface? | 2 | 1 | 3 | 1 |
| 7. | Explain page table in virtual memory. | 2 | 2 | 4 | 1 |
| 8. | How is data stored and retrieved in optical disks. | 2 | 1 | 4 | 1 |
| 9. | What is Super Scalar operation? How is it different from a pipeline? | 2 | 1 | 5 | 1 |
| 10. | Discuss the effect of complex addressing modes in a pipeline. | 2 | 2 | 5 | 1 |
| | ***Part-B (5 × 8 = 40 Marks)*** | | | | |
| 11. a) | A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of the 64 registers, and an address part.<br>a. How many bits are there in the operation code, the register code part, and the address part?<br>b. Draw the instruction word format and indicate the number of bits in each part.<br>c. How many bits are there in the data and address inputs of the memory? | 4 | 3 | 1 | 2 |
| b) | Write code for the following equation using Two address instruction format and One address instruction format.<br>(A + B) - (C * D) | 4 | 3 | 1 | 2 |
| 12. a) | In the selective complement operation, what is the logical microoperation used. what is the value of B if $A_t$ = 1 1 0 0 and $A_{t+1}$ = 0 1 1 0. In the selective set operation, what is the logical microoperation used. what is the value of B if $A_t$ = 1 1 0 0 and $A_{t+1}$ = 1 1 1 0. | 4 | 3 | 2 | 1 |

*Contd... 2*

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|---|---|---|---|---|---|
| b) | Write a Microprogram control sequence to fetch an instruction from memory, if the memory is byte addressable and the word size is 32 bits. If the instruction fetched is "INC R1" write control signals for execution of the instruction. | 4 | 3 | 2 | 2 |
| 13. a) | Draw block diagram of DMA controller. Explain the role of DMA controller in DMA transfer specifically mentioning the order of communication among I/O interface, CPU and memory. | 4 | 2 | 3 | 1 |
| b) | A computer has interfaces for its I/O devices. The device and its priority and vector address are given in the following table. Develop and draw a suitable block diagram showing daisy chain priority interrupt. | 4 | 3 | 3 | 2 |
| 14. a) | Compare the different types of semiconductor RAM memories. How do they differ from ROM. | 4 | 2 | 4 | 1 |
| b) | A computer has a main memory of size 1M and a direct mapped cache of size 1K. Each block of cache can store 128 words. How many bits are there in the TAG, BLOCK and WORD fields. Draw and illustrate the positioning of the following main memory blocks in the cache memory blocks.<br>Main memory block Numbers: 167, 45, 32, 98, 257. | 4 | 3 | 4 | 2 |
| 15. a) | Define Pipeline. Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks? | 4 | 1 | 5 | 1 |
| b) | A six-stage pipeline has the stage delay of 140, 170, 160, 130, 180, 150 n secs, respectively. Registers that are used between stages have a delay of 10 n secs each. Assuming a constant clock rating, what is the total time taken by pipeline for 1000 tasks? What is the speed up achieved using the pipeline? | 4 | 3 | 5 | 2 |
| 16. a) | For the following addressing modes, write advantage and disadvantage of each.<br>a) Direct addressing mode. b) Indirect addressing mode.<br>c) Register addressing mode. d) Immediate addressing mode. | 4 | 1 | 1 | 1 |
| b) | Explain with a diagram, an adder-subtractor combinational circuit. | 4 | 2 | 2 | 1 |
| 17. | Answer any ***two*** of the following: | | | | |
| a) | Explain the handshake control of data transfer during input and output operation. | 4 | 2 | 3 | 1 |
| b) | Explain cache set associative mapping technique. Compare its advantages and disadvantages with direct mapping and associative mapping. | 4 | 2 | 4 | 1 |
| c) | Discuss the types of hazards in a pipeline. Suggest one solution for each type. | 4 | 2 | 5 | 1 |

| Device | Priority | Vector Address |
|---|---|---|
| Magnetic Disk | High | Ox1000H |
| Printer | Medium | Ox2000H |
| Keyboard | Low | Ox3000H |

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

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|---|---|---|
| i) | Blooms Taxonomy Level – 1 | 20% |
| ii) | Blooms Taxonomy Level – 2 | 40% |
| iii) | Blooms Taxonomy Level – 3 & 4 | 40% |

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